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6. What problems do non-linear loads and harmonics create?

Most power systems can accommodate a certain level of harmonic currents but will experience problems when they become a significant component of the overall load. As these higher frequency harmonic currents flow through the power system, they can create problems such as:

- Overheating of electrical distribution equipment, such as cables, transformers, standby generators, etc.
- Overheating of rotating equipment, such as electric motors
- High voltages and circulating currents caused by harmonic resonance
- Equipment malfunctions due to excessive voltage distortion
- Increased internal losses in connected equipment resulting in component failure and shortened lifespan
- False operation of protection equipment
- Metering errors
- Lower system power factor preventing effective utilization
- Voltage regulator problems on diesel generators
- Inability of automatic transfer switches to operate in closed transition

Harmonics overheat equipment by several means. For example, in electric machines and transformers, harmonic currents cause additional power losses by (i) increasing the eddy currents that flow in their laminated cores, (ii) through increased leakage currents across insulation and (iii) by producing skin effect in conductors. For additional information on how harmonics increase power losses and overheat transformers see Question 10.

The incidence of hot transformers and neutral conductors has been especially common. Even under less than full load conditions, a transformer can run surprisingly hot. One of the reasons is its winding configuration. The overwhelming majority of distribution transformers are DELTA primary, GROUNDED WYE secondary. The delta winding has some undesirable characteristics when significant amounts of 3rd harmonic (and other zero sequence currents) are present on the load side. These harmonics return along the neutral conductor and are trapped in the primary DELTA winding where they circulate causing significant extra heating. They do not flow through to the primary system, but they also are NOT cancelled (Figure 6-1).

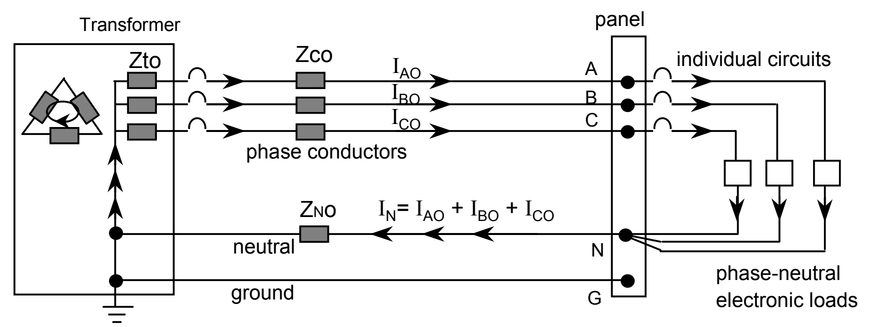

Figure 6-1: Zero sequence currents trapped in the transformer's delta winding

Since additional heating will reduce the life-span of a transformer, it must either be derated (not operated at its full nameplate rating), built to tolerate this additional heating (K-rated transformer) or designed to prevent the primary side circulating currents from being induced (harmonic mitigating transformer). A guide for derating has been proposed by CBEMA (Computer and Business Equipment Manufacturers Association) with the intent to provide users the ability to protect existing transformers which service non-linear loads. The relationship is as follows:

Derating Factor = (1.414 x RMS load current) / (PEAK load current)

Since many of today's multimeters can measure both peak and TRUE-RMS current, the derating factor can be quickly calculated. When a transformer feeds personal computers and other electronic equipment, typical values range from 0.5 to 0.7 meaning that the transformer should be loaded no more than 50 - 70% of its nameplate full-load rating to prevent damage due to premature aging.

The fact that harmonic currents create voltage distortion as they flow through the power system's impedance makes their impact even more serious. It is voltage distortion, not current distortion, that will affect the connected equipment on the power system. For more on how non-linear loads create voltage distortion and how this can affect connected equipment, see Questions 8 and 9.

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7. Why do 3rd harmonic currents overload neutral conductors?

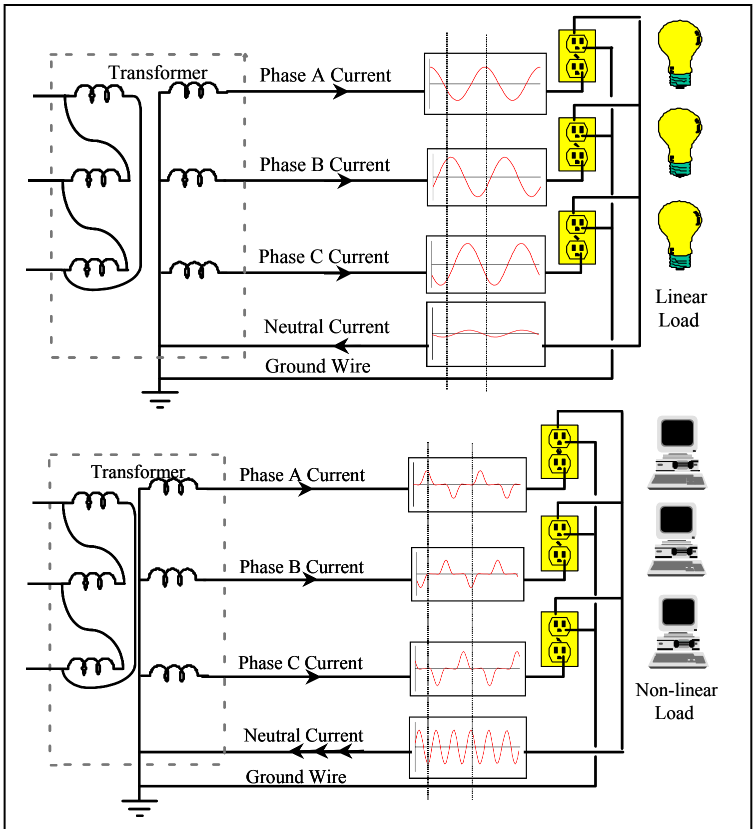

Figure 7-1: How non-linear load currents add in the neutral

Figure 7-1 shows how the sinusoidal currents on the phases of a 3-phase, 4-wire system with linear loads sum to return on the neutral conductor. The 120° phase shift between the sinusoidal load currents causes their vector sum to be quite small. In fact it will be zero if the linear loads are perfectly balanced.

Examining the dashed vertical lines in Figure 7-1 clearly demonstrates that the instantaneous sum of the currents in the three phases taken at any moment will also be zero if the linear loads are perfectly balanced. If they are not, then there will be a small residual neutral current as shown.

With linear loads, the neutral conductor can be the same size as the phase conductors because the neutral current will not be larger than the highest phase current. Unfortunately, this is definitely not true for non-linear phase-to-neutral loads.

120VAC non-linear loads like the SMPS used in computers and in monitors draw current in two distinct pulses per cycle. Because each pulse is narrow (less than 60 degrees), the currents in the second and third phases are zero when the current pulse is occurring in the first phase. Hence no cancellation can occur in the neutral conductor and each pulse of current on a phase becomes a pulse of current on the neutral.

Even if the phase currents of the SMPS loads are perfectly balanced in RMS amperes, the RMS value of the neutral current can be as much as √3 times the RMS value of the phase current because there are 3 times as many pulses of current in the neutral than in any one phase. If the phase current pulses do overlap because they exceed 60 degrees in width, then there will be some cancellation so that the neutral current will be less than √3 times the phase current. Overlapped or not, because there are 3 times as many pulses in the neutral than in a phase, the predominant component of the neutral current will be the 3rd harmonic (180Hz for a 60Hz system). This is evident in the waveforms of Figure 7-1 since the linear current completes only 2 cycles in the same time period that the non-linear neutral current completes 6 cycles or 3 times the fundamental.

Often, in new construction this situation is addressed by simply doubling the neutral conductor ampacity. In existing facilities however, it is most often very difficult and too costly to implement this solution, therefore an alternate method is usually necessary. Question 11 describes how Zero Sequence Harmonic Filters can be used very effectively to reduce 3rd harmonic currents in the neutral conductor.

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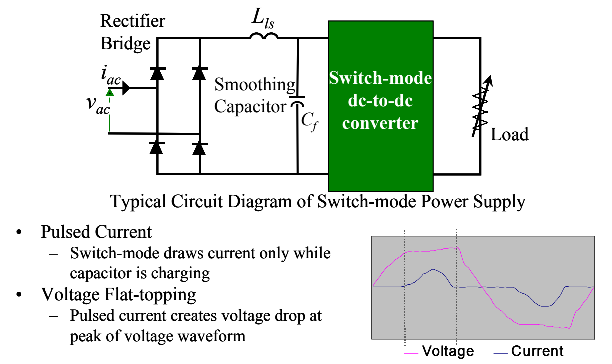
8. How do non-linear loads create current and voltage harmonics?

The switch-mode power supply (SMPS), used in most digital electronic equipment, is an excellent example of a non-linear load. Because it draws current in non-sinusoidal pulses, the SMPS is a significant generator of harmonic currents. When found in high densities multiple SMPS can be a major contributor to voltage distortion. Figure 8-1 shows how the pulsed current consumed by a single-phase SMPS will produce voltage distortion in the form of flat-topping. Since current is consumed only at the peak of the voltage waveform (to charge the smoothing capacitor), voltage drop due to system impedance will also occur only at the peak of the voltage waveform. A flattened voltage peak will reduce the DC bus voltage of the SMPS, reduce its power disturbance ride-through capability, and increase both its current draw and I^2R losses.



Typical Circuit Diagram of Switch-mode Power Supply

- Pulsed Current
  - Switch-mode draws current only while capacitor is charging
- Voltage Flat-topping
  - Pulsed current creates voltage drop at peak of voltage waveform

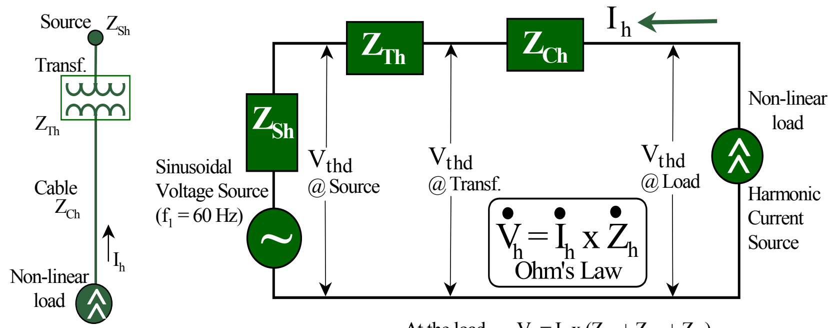
Figure 8-1: Switch-mode Power Supply and Voltage Flat-topping

Another way to analyze the operation of the system with non-linear loads is to calculate the effect of each individual harmonic current as it flows through the various impedances of the distribution system. Fourier analysis tells us that the 2-pulse current drawn by the SMPS rectifier has a fundamental frequency component plus all of the odd harmonics (3rd, 5th, 7th, 9th, 11th, etc.) When modeling the distribution system, we can think of each SMPS as a generator of harmonic currents. Each harmonic current injected into the power system by a non-linear load will flow through the system impedance, resulting in a voltage drop at that harmonic frequency. The amount of voltage drop follows Ohm's Law ($V_h = I_h$ x Z_h) where:

V_h = voltage at harmonic number h
I_h = amplitude of current harmonic h
Z_h = impedance of the system to harmonic h.

Figure 8-2 shows the relationship between system impedance and the voltage and current distortion components at several points in a typical power system.

We can calculate the RMS value of the voltage or current distortion if we know the RMS values of all of the components. Parseval's Theorem tells us that the RMS value of a waveform is equal to the square root of the sum of the squares of the RMS values of the fundamental component and all of the harmonic components of the waveform.



Where,
V_h = hth harmonic voltage
I_h = hth harmonic current
Z_h = Impedance at hth harmonic
V_{thd} = Voltage total harmonic distortion

At the load, $V_h = I_h \text{ x } (Z_{Ch} + Z_{Th} + Z_{Sh})$
At the transf., $V_h = I_h \text{ x } (Z_{Th} + Z_{Sh})$
At the source, $V_h = I_h \text{ x } (Z_{Sh})$

$$V_{thd} = \frac{\sqrt{V_2^2 + V_3^2 + ... + V_h^2}}{V_1} \text{ x } 100\%$$

Figure 8-2: Relationship between System Impedance and Voltage Distortion

The fundamental is not a distortion component, so the RMS value of the distortion is just the square root of the sum of the squares of the harmonic components. Usually this is expressed as percentage of the value of the fundamental component and is called the *Total Harmonic Distortion*, or *THD*.

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Voltage total harmonic distortion (V_{thd}) is calculated as:

$$V\,thd = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + \ldots}}{V_1} \times 100\%$$

Similarly, current total harmonic distortion is calculated as:

$$I\,thd = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + I_5^2 + \ldots}}{I_1} \times 100\%$$

Voltage distortion then is a function of both the system impedance and the amount of harmonic current in the system. The higher the system impedance (ie. long cable runs, high impedance transformers, the use of diesel generators or other weak sources) the higher the voltage distortion.

In Figure 8-2, we see that voltage distortion is greatest at the loads themselves, since the harmonic currents are subjected to the full system impedance (cables, transformer and source) at that point. This is a characteristic most often misunderstood. It means that even if voltage distortion levels are low at the service entrance, they can be unacceptably high at the loads themselves. It also emphasizes the importance of keeping system impedances relatively low when servicing non-linear loads.

Voltage distortion can be minimized by removing the harmonic currents (I_h) and/or lowering the system impedance (Z_h) to the harmonics. (For further information on the relationship between voltage drop and voltage distortion and how to minimize them, we recommend two MIRUS technical papers titled (1) "*Taming the Rogue Wave – Techniques for Reducing Harmonic Distortion*" and (2) *"How the Harmonic Mitigating Transformer Outperforms the K-Rated Transformer"*). For information on how Harmonic Mitigating Transformers reduce voltage distortion see Question 13.

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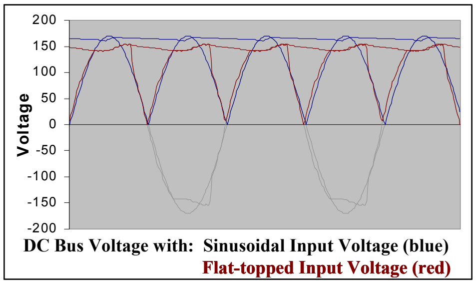
9. What ill effects do harmonics created by the computer power supplies have on themselves?

As voltage becomes more and more distorted, it will begin to have a negative effect on the connected equipment. A flat-topped voltage waveform can affect a switch-mode power supply (SMPS) in at least 2 major ways:

- A reduced peak voltage will translate to a lower DC bus voltage in the SMPS. Input current to the SMPS will increase because the computer or other electronic load still requires the same amount of power. Increased I^2R losses in the SMPS accelerate the aging of its components.
- Power disturbance ride-through capability is reduced since the reduced peak voltage means the large filter capacitor on the DC bus of the SMPS will be able to store much less energy.

When an SMPS is supplied by a voltage waveform with a flattened peak (red trace in Figure 9.1) rather than a nearly pure sinusoidal voltage (blue trace), the DC bus voltage is reduced proportionately (red trace). With a lower DC bus voltage, the SMPS will need to draw more current in order to deliver the same amount of power required by the load (I = P/V). This increase in current will result in increased component heating from higher I^2R losses and a reduced life expectancy of the components due to their higher operating temperature. For example, a 10% decrease in peak voltage (from 169V to 153V) will increase the SMPS line current by about 11% which will in turn increase the I^2R portion of the SMPS losses by about 23%. The correlation of SMPS failures with increased voltage distortion is usually subtle because equipment aging takes time to accumulate.

The first purpose of the large filter capacitor on the DC bus of an SMPS is to reduce the voltage ripple. The second purpose is to support its electronic load during a power disturbance that produces a momentary power interruption or major power dip. Since a typical SMPS is capable of operating for short periods at voltage levels as low as 70%, we can calculate the reduction in ride-through time if the initial voltage stored in the capacitor is below its rated peak voltage. For instance, if the peak voltage supplied to the SMPS is flat-topped by 30%, the ride-through capability is essentially zero and the I^2R losses are twice those present at rated peak voltage.



- Voltage flat-topping reduces DC bus voltage
- Lower DC voltage, increases current and I^2R losses (heat)
- Pre-mature component failure results from higher operating temperatures

10% drop in peak voltage produces

11% increase in current and

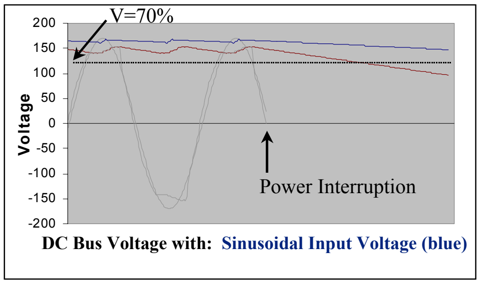
23% increase in I^2R losses

$$P = V\,I$$

$$\text{If } V = 0.9 \text{ pu},\quad I = \frac{P}{V} = \frac{1.0}{0.9} = 1.11 \text{ pu}$$

$$P_{Loss} = I^2R = (1.11)^2\,(1) = 1.23 \text{ pu}$$

Figure 9-1: How voltage flat-topping affects DC bus voltage and equipment over-heating



- Voltage flat-topping reduces DC bus voltage
- Lower charging voltage on smoothing capacitor, reduces stored energy
- With less stored energy ride-through capability is reduced

10% drop in peak voltage reduces ride-through capability by 37%

Energy recovered from capacitor during ride-through: $W_R = 1/2\, C\,(V_1^2 - V_2^2)$

With drop-out voltage = 70% (V_2 = 0.7 pu)

$V_1 = 1$ pu,	$V_1 = 0.9$ pu
$W_R = (1^2 - 0.7^2)$ $= 0.51$ pu	$W_R = (0.9^2 - 0.7^2)$ $= 0.32$ pu

$$\frac{(0.51 - 0.32)}{0.51} \times 100\% = 37\%$$

Figure 9-2: How voltage flat-topping affects equipment ride-through capability

With the correct initial peak voltage, the stored energy in the capacitor will often provide several cycles of ride-through capability before its voltage is reduced to 70% of nominal. This is dramatically reduced however, when the SMPS supply voltage is flat-topped because the energy stored in the capacitor is proportional to the square of the voltage. Figure 9-2 shows how a 10% reduction in the peak voltage supplied to computer equipment will reduce the power dip ride-through time by about 37%. Without the correct peak voltage, the smoothing capacitor in the SMPS will not be fully charged. Initially lower stored energy means that the capacitor will support the load for a much shorter period during a power interruption. When voltage flat-topping becomes severe enough, brief power interruptions such as those characterized by the lights flickering, will begin to affect equipment that would otherwise be unaffected.

In order to ensure reliable operation of power electronic equipment as well as other equipment on the power system, it is important to simultaneously maintain the correct level of both RMS voltage and peak voltage. This can best be achieved by using harmonic mitigation equipment that minimizes voltage distortion throughout the system by removing the harmonic currents from interacting with the upstream supply and distribution equipment.

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10. How do harmonics increase power losses and overheat transformers?

Harmonics generated by non-linear loads substantially increase the losses in conventional or K-rated delta-wye distribution transformers. This increase in losses will increase operating costs and can shorten transformer life. The main thrust of the K-rated design is not to lower the increased losses caused by harmonics but rather to withstand them without overheating.

Transformer loss components include no load (P_{NL}) and load losses (P_{LL}). The no load losses are transformer core losses. They depend mainly upon the peak flux levels reached in the core so the increase in no load losses due to harmonics is usually negligible. On the other hand, load losses are significantly increased by harmonic currents created by non-linear loads.

Load losses consist primarily of I^2R copper losses (P_R) and eddy current losses (P_{EC}). Harmonics increase these losses in the following ways:

1. Copper Losses, I^2R
   Harmonic currents are influenced by a phenomenon known as skin effect. Since they are of higher frequency than the fundamental current they tend to flow primarily along the outer edge of a conductor. This reduces the effective cross sectional area of the conductor and increases its resistance. The higher resistance will lead to higher I^2R losses.

2. Eddy Current Losses
   Stray electromagnetic fields will induce circulating currents in a transformer's windings, core and other structural parts. These eddy currents produce losses that increase substantially at the higher harmonic frequencies. The relationship is as follows:

$$P_{EC} = P_{EC-1} \sum_{h=1}^{h_{\max}} I_h^2 h^2$$

Where:
P_{EC} = Total eddy current losses
P_{EC-1} = Eddy current losses at full load based on linear loading only.
I_h = rms current (per unit) at harmonic h
h = harmonic #

For linear loads, eddy currents are a fairly small component of the overall load losses (typically about 5%). With non-linear loads however, they become a much more significant component, sometimes increasing by as much as 15x to 20x. A transformer can easily be subjected to losses exceeding its full load rating even though the RMS value of the non-linear load current indicates only partial loading.

Because Harmonic Mitigating Transformers (HMT) cancel certain harmonic fluxes without coupling them to the primary windings, their primary winding currents are lower than those found on conventional transformers having the same level of non-linear load currents on the secondary side. This means that the I^2R losses and eddy current losses on the primary of an HMT are considerably reduced compared to those in a conventional transformer.

The conventional and k-rated delta-wye transformers have the same level of 3rd, 5th, 7th, and 9th harmonic currents in their primary windings as in their secondaries. Do not be misled by the low level of triplen harmonics in the feeder conductors to a delta-wye transformer. Checking the delta primary winding itself will show that the same percentage of 3rd and 9th harmonic currents (compared to the fundamental current) are circulating in the delta primary as is present on the wye secondary. This increases the losses and voltage distortion on a delta-wye transformer compared to an HMT.

Checking the primary of an HMT will reveal only residual amounts of 3rd and 9th harmonic current. Even better, checking the primary of a dual output HMT (MIRUS Harmony-2 for example) will show only residual amounts of 3rd, 5th, 7th, and 9th. Hence lower harmonic losses and lower voltage distortion when HMTs are used to feed non-linear loads.

References:
1. Thomas S. Key, *Costs and Benefits of Harmonic Current Reduction for Switch-Mode Power Supplies in Commercial Office Building,* IEEE Transactions on Industry Applications, Vol. 32, No. 5 Sept/Oct 1996, pp. 1017-1024
2. ANSI/IEEE C57.110-1986, Recommended Practice for Establishing Transformer Capability When Supplying Nonsinusoidal Load Currents, American National Standards Institute